REMARKS

Responsive to the Office Action mailed February 21, 2007, Applicants provide the following. Claims 4, 11, 17, 26, 39, 45, 52, 53 and 55 have been amended, claims 5, 12-13, 18, 27 and 40 have been canceled, claims 6-9, 28-31 and 51 were previously canceled, and new claims 60-65 have been added. Therefore, fifty (50) claims remain pending in the application: claims 1-4, 10-11, 14-17, 19-26, 32-39, 41-50 and 52-65. Reconsideration of claims 1-4, 10-11, 14-17, 19-26, 32-39, 41-50 and 52-65 in view of the amendments above and remarks below is respectfully requested.

By way of this response, Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain any outstanding issues that require adverse action, it is respectfully requested that the Examiner telephone the undersigned at (858) 552-1311 so that such issues may be resolved as expeditiously as possible.

Finality of Office Action

1. Applicants respectfully submit that the finality of the Office Action mailed February 21, 2007 is in error. Following the Appeal Brief filed on November 17, 2006, prosecution has been reopened and the Examiner has set forth new grounds for rejecting all of the claims pending in the application. Many of the applied references are newly applied references not previously cited by the Applicants in an Information Disclosure Statement, or cited in any previous Office Action. Applicants have not submitted amendments to the claims following the final office action of May 5, 2006 or in the appeal brief filed November 17, 2006 that overcame the prior rejections.

MPEP section 1207.04 states that "[t]he Office action containing a new ground of rejection may be made final if the new ground of rejection was (A) necessitated by amendment, or (B) based on information presented in an information disclosure statement." As stated above, the rejections of the claims of the present Application based on the new references applied in the present Office Action are not necessitated by an amendment as no amendment was made to the claims. Further the

newly applied references were not listed in a previous Information Disclosure Statement filed by Applicants and were not previously cited by the Office during the prosecution of the subject application. As a result, Applicants have not had a proper opportunity to respond to these references. Therefore, the new grounds for rejection were not "necessitated by amendment, or (B) based on information presented in an information disclosure statement" (MPEP 1207.04), and thus, Applicants respectfully submit that the finality of the present Office Action is in error and request that the finality of the present Office Action be withdrawn.

Claim Rejections - 35 U.S.C. § 103

2. Claims 1-5, 10, 11, 16, 17, 19-27, 32, 33, 38, 39, 41-48, 50 and 52-59 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,699,384 (Dillon) in view of U.S. Patent No. 6,005,565 (Legall et al.), U.S. Patent No. 5,301,279 (Riley et al.) and U.S. Patent No. 5,982,363 (Naiff). Applicants respectfully traverse these rejections in that one skilled in the art would not combine the references and the applied combination of references fail to teach or suggest each limitation as recited in at least amended independent claims 1, 23 and 45.

Applicants respectfully submit that one skilled in the art would not combine at least the Riley patent with the Dillon patent. Specifically, the Dillon patent describes an adaptor card that is specifically designed to receive satellite communications and forwarding those communications to the CPU of a computer. Further, the card system described in Dillon is specifically designed to forward the satellite communication without adding the complexity or altering the computer while still accurately supplying the satellite communications. It would defeat the purpose of provide a personal computer with the ability to receive satellite communication if the computer were further required to have additional buffers to achieve the communication. Dillon is specifically designed to provide the satellite communications through an adaptor card without the need for additional buffering on the computer or the bus. One skilled in the art when referencing the Dillon patent would not refer to the Riley patent

as the buffering described by Riley is not needed, provides no benefit and instead adds complexity and cost without benefit. Therefore, one skilled in the art would not incorporate the buffering of Riley into the system of Dillon.

Further, the adaptor card of Dillon is configured to rapidly response to user requests to tune in a selected content. Dillon defines how the CPU 120 instructs the adaptor card 124 to tune in a users selected frequency. Dillon specifically states that "CPU 120 controls tuner 132 by passing control data via [the bus 135 to] bus interface 134" so that the "[t]uner 132 selects one of the analog signals in accordance with a tuning frequency previously sent to tuner 132 by CPU 120" (Dillon, col. 4, lines 11-17). However, the Riley patent specifically limits the transfer of data from the computer system through buffer system such that "Before information can be written from the channel buffer to the peripheral device, 32 bits of information must first be read from the memory 20 into the channel buffer across the internal bus 22" (Riley, col. 9, lines 58-62). Therefore, the buffering system prevents communication until 32 bits of information are to be transferred. This could significantly delay communications from being received at the tuner and significantly degrade performance of the system. Therefore, one skilled in the art would not incorporate the buffering system of Riley into the adaptor card system of Dillon as it would degrade the operation of the adaptor card, and would not provide any apparent benefit.

Additionally, Applicants respectfully submit that the benefits of incorporating the buffer logic circuit as recited in claim 1 and at least the buffering provided by the buffer logic circuit recited in claim 1 are only appreciated through the benefit of hindsight provided by the present application. Therefore, combining the buffers of Riley with adaptor card of Dillon would at best, if arguendo one combined Riley with Dillon, would only be apparent by applying impermissible hindsight, and thus, Applicants respectfully request the rejection be withdrawn.

Independent claim 23 is also not obvious over the applied combination of Dillon, Naiff, Legall and Riley. As introduced above, one skilled in the art would not

combine at least Dillon with Riley as demonstrated above, as such combination would require added complexity with no benefit as the Dillon patent provides already provides the satellite communications to the CPU of the personal computer without the need of the added complexity of bus buffers as described in Riley, and the buffering system described in Riley would be detrimental to the operation of the adaptor card of Dillon. Therefore, claim 23 is not obvious in view of the applied combination.

Amended independent claim 45 is also patentable over the applied combination of the Dillon, Naiff, Legall and Riley patents because one skilled in the art would not combine the applied references and the applied combination fails to teach each limitation as recited in pending claim 45.

As demonstrated above, one skilled in the art would not combine at least the Riley patent with the Dillon patent as there is no apparent benefit, and instead would require the altering of the personal computer into which the adaptor card could be used, the added complexity and cost to the personal computer to incorporate the buffers onto the peripheral bus, without an apparent benefit as the adaptor card of Dillon already is configured to supply the satellite communications to the CPU of the personal computer. Further, the buffering system of Riley would be detrimental to the operation of the adaptor card of Dillon. Therefore, one skilled in the art would not combine Riley with Dillon, and thus, claim 45 is not obvious in view of the applied combination.

Further, the applied combination of references fails to teach or suggest at least an Internet processing element that comprises first video processor and a buffer logic circuit that also comprises a second video processor as well as a multiplexer coupled with both the first and second video processor. There is not teaching or suggestion in applied combination that both the Internet processing element and the buffering logic circuit include video processors.

Furthermore, the combination does not teach or suggest that the multiplexer receives "at least a portion of the sensory data and directs the portion of the sensory data to one of the first and second video processors to conditionally process the

portion of the sensory data" as recited in amended claim 45. There is no teaching or suggestion in the combination of Dillon, Naiff, Legall and Riley to provide a buffer logic circuit with a multiplexer that directs sensory data to one of a second video processor of the buffer logic circuit or to a first video processor of the Internet processing element. Thus, the applied combination does not teach or suggest each limitation as recited in claim 45 and therefore, claim 45 is patent over the applied combination.

Claims 2-4, 10-11, 16-17, 19-22, 53-54 and 57-62 depend from independent claim 1; claims 24-27, 32-33, 38-39, 41-44 and 55-56 depend from independent claim 23; and claims 46-48, 50, 52 and 63-63 depend from independent claim 45. Therefore, claims 2-4, 10-11, 16-17, 19-22, 24-27, 32-33, 38-39, 41-44, 46-48, 50 and 52-63 are patentable over the applied combination of Dillon, Naiff, Legall and Riley due at least to their dependency on allowable claims 1, 23 and 45.

Further regarding at least claim 52, the applied combination fails to teach or suggest that the buffer logic receives both digital communication signals received from the DSS processing element and broadcast data that is forwarded to the Internet processing element. In rejecting claim 52 the office action cites Dillon at column 4, lines 8-21 which is the same section cited in rejecting claim 45 suggesting that Dillon teaches a buffer that facilitates the transfer of "digital signals between the DSS processing element and the computer circuit" (office action, pg. 9). Therefore, the office action has equated the digital signals claimed in claim 45 as well as the broadcast data received by the buffer logic as the same content, effectively reading the broadcast content out of the claim and ignoring this limitation. The broadcast data is a separate limitation distinct from the digital signals received from the DSS processing element. There is no discussion or suggestion in the Dillon patent or in the applied combination that the bus 135 of Dillon receives broadcast data as recited in claim 52. Therefore, the applied combination fails to teach each limitation as recited in claim 52, and claim 52 is patentable over the applied combination.

Further, claim 52 was amended to clarify that the broadcast data is received by the buffer logic "in addition to the digital communication signals received from the DSS processing element" (claim 52). This amendment was not necessitated for reasons of patentability or to overcome rejections, but instead was added to clarify the claim language. There is not teaching or suggestion that the applied combination teaches a buffer logic that receives both broadcast data and digital communication signals. Thus, claim 52 is not obvious over the applied combination of references and is patentable over the applied combination.

Dependent claims 53-56 and 62-63 similarly recite that buffer logic receives broadcast data in addition to digital signals from the circuit that received wireless television communication signals or the DSS processing element. Therefore, similar arguments as presented for claim 52 can be presented for claims 53-56 and 62-63, and thus, claims 53-56 and 62-63 are also patentable over the applied combination of references.

Regarding at least claim 57, Applicants respectfully submit that the applied combination fails to teach or suggest at least an option palette "that displays a calendar indicating programs that are selected" as recited in claim 57. The office action in rejecting claim 57 cites Figure 2 of the Legall patent. However, the Legall patent does not show or suggest at least an option palette with a calendar, or a calendar showing selected programs. Instead, Figure 2 of Legall only shows an electronic programming guide 220 that displays a single channel for a one and a half hour period of time. There is no teaching or suggestion in Legall to provide and option palette that comprises a calendar indication of programs, or a calendar indicating programs that are selected. The Dillon, Naiff and Riley patents also fail to teach or suggest an option palette as recited in claim 57. Therefore, claim 57 is also patentable over the applied combination of references.

Claim 58 is also patentable over the applied combination of references. For example, the applied combination of references fails to teach or suggest a buffer logic circuit that comprises "a multiplexer coupled with a plurality of buffers" as recited

in claim 58. The office action in rejecting claim 58 suggests that multiplexers are inherent in the Riley patent. Specifically, the office action suggests that multiplexing are "inherent steps for routing data between the processor complex and the peripheral devices..." (office action, pg. 15). Applicants respectfully traverse this assertion.

Instead, the Riley patent fails to describe or suggest multiplexers and instead describes signaling from the IOCC 14 that dictates the communication of at least the data from the buffers to the peripheral devices such that devices are notified through commands. For example, Riley describes that the IOCC 14 dictates the communication to and from the buffers, and further dictates when peripheral devices are granted access to at least the peripheral bus, where the IOCC 14 generates a "a -PHLDA (peripheral hold acknowledge) signal which is activated at time 128 and generated from the IOCC 14 to the peripheral device acknowledging the grant of the peripheral bus 36 access" (Riley, col. 9, lines 48-53). The Riley patent continues stating that "[s]ince the peripheral bus 36 is now in a state where data transfer may commence, line 130 within the IOCC 14 provides a -PWR (peripheral write) signal which is a write strobe for the peripheral device. The -PWR signal is activated at time 132 to start the operation" (Riley, col. 9, lines 53-57). Therefore, it is clear that the IOCC dictates the communication to and from the buffers by granting access the peripheral bus to specific peripheral devices.

Further, the IOCC 14 identifies the buffers, memory and or peripheral device where "the IOCC 14 will provide appropriate address instructions as indicated by a SADR/PADR signal on the line 174" (Riley, col. 10, lines 49-51). Therefore, the IOCC defines the addressing and dictates which peripheral device has access to the peripheral bus, and thus, multiplexers are not utilized by the Riley and not inherent as suggested by the office action, and instead, Riley specifically teaches away from the use of multiplexers as claimed because the IOCC provides the functionality without the added circuitry of the multiplexers. Thus, the applied combination does not teach or suggest, and instead teaches away from the buffers and multiplexers as recited in claim 58, and claim 58 is patentable over the applied combination.

Claim 59 depends from claim 58, and thus, claim 59 is also allowable over the applied references due to its dependency on allowable claim 58. Further, the office action suggests that it is inherent in Riley to include address decoders as claimed. However, as demonstrated above, the IOCC provides addressing and thus address decoders are not needed. Thus, claim 59 is allowable over the applied combination of Dillon, Naiff, Legall and Riley.

3. Claims 18 and 40 stand rejected under 35 U.S.C. § 103(a), as being unpatentable over Dillon, Naiff, Legall and Riley in further view of U.S. Patent No. 5,081,628 (Maekawa et al.). Claim 18 depends from claim 1, and claim 40 depends from claim 23. Applicants have demonstrated above that independent claims 1 and 23 are not obvious in view of the combination of Dillon, Naiff, Legall and Riley. Maekawa also fails to teach or suggest at least a buffer logic circuit or buffering as recited in claims 1 and 23, and one skilled in the art would not combine at least Riley with Dillon. Therefore, claims 18 and 40 are also not obvious over the combination of references for at least the reasons provided above.

4. Claims 12, 13, 34 and 35 stand rejected under 35 U.S.C. § 103(a), as being unpatentable over Dillon, Naiff, Legall and Riley in further view of U.S. Patent No. 6,208,384 (Schultheiss). Claims 12 and 13 depend from claim 1, and claims 34 and 35 depend from claim 23. As demonstrated above, claims 1 and 23 are patentable over the combination of Dillon, Naiff, Legall and Riley. Schultheiss also fails to teach at least the buffer logic circuit and buffering as recited in claims 1 and 23. Therefore, claims 12, 13, 34 and 35 are also not obvious over the applied combined references.

5. Claims 14, 15, 36, 37 and 49 stand rejected under 35 U.S.C. § 103(a), as being unpatentable over Dillon, Naiff, Legall and Riley and in further view of U.S. Patent No. 6,216,264 (Maze et al.). Claims 14 and 15 depend from claim 1, claims 36 and 37 depend from claim 23 and claim 49 depends from claim 45. As demonstrated

above, claims 1, 23 and 45 are patentable over the applied combination. Maze also fails to teach at least the buffer logic and buffering as recited in claims 1, 23 and 45. Therefore, claims 14, 15, 36, 37 and 49 are also not obvious over the combined references for at least the reasons provided above.

NEW CLAIMS

6. New claims 60-63 depend from claim 1, claim 64 depends from claim 23 and new claim 65 depends from claim 45. Therefore, claims 60-65 are also patentable over the applied references due at least to their dependency on allowable claims 1, 23 and 45.

Further, new claim 60 recites, for example, that the buffer logic circuit comprises first and second multiplexers as well as first and second narrowband buffers and third wideband buffer. The combination of Dillon, Naiff, Legall and Riley does not teach or suggest the multiplexers or the three buffers as recited. The office action in rejecting claim 1 suggests that Dillon describes a buffer logic circuit citing a bus 135 of Dillon, but admits that the combination of Dillon Naiff and Legall fails to describe buffering data or buffers. Instead, the office action relies on Riley to suggest that the combination describes buffers. Applicants respectfully submit that one skilled in the art would not combine the buffers of Riley with the adaptor card of Dillon as demonstrated above. Further, Riley fails to teach or suggest at least first and second narrowband buffers, and also fails to suggest a third wideband buffer.

Instead, Riley teaches away from such a configuration of buffers. Specifically, Riley describes a buffer associated with each peripheral device where these buffers "temporarily store data in thirty-two (32) bit wide quantities for transfers between the respective peripheral devices 24, 26 and 28" (Riley, col. 5, lines 32-38). Therefore, Riley specifically requires each peripheral device be cooperated with a buffer, and that the buffer be specific to provide thirty-two bit wide transfers. Further, Riley specifically describes that to achieve the intended implementation and performance data is transferred from buffers in thirty-two bit wide transfers only once the buffers are full

(see Riley, col. 6, lines 7-8), and thus, teaches away from having narrowband and wideband buffers.

Still further, the Riley patent fails to teach or suggest multiplexers or first and second multiplexers as recited in claim 60. The office action in rejecting claim 58 suggests based on Riley that it is "inherent steps for routing data between the processor complex and the peripheral devices..." (office action, pg. 15). Applicants respectfully traverse this assertion. Instead, Riley fails to describe multiplexers and instead describes signaling from the IOCC 14 that dictates the communication of at least the data from the buffers to the peripheral devices such that devices are notified through commands. Specifically, Riley describes that the IOCC 14 dictates the communication to and from the buffers, and further dictates when peripheral devices are granted access to at least the peripheral bus, where the IOCC 14 generates a "a -PHLDA (peripheral hold acknowledge) signal which is activated at time 128 and generated from the IOCC 14 to the peripheral device acknowledging the grant of the peripheral bus 36 access" (Riley, col. 9, lines 48-53). The Riley patent continues stating that "[s]ince the peripheral bus 36 is now in a state where data transfer may commence, line 130 within the IOCC 14 provides a -PWR (peripheral write) signal which is a write strobe for the peripheral device. The -PWR signal is activated at time 132 to start the operation" (Riley, col. 9, lines 53-57). Therefore, it is clear that the IOCC dictates the communication to and from the buffers by granting access the peripheral bus to specific peripheral devices.

Further, the Riley patent describes that the IOCC 14 identifies the buffers, memory and or peripheral device where "the IOCC 14 will provide appropriate address instructions as indicated by a SADR/PADR signal on the line 174" (Riley, col. 10, lines 49-51). Therefore, the IOCC defines the addressing and dictates which peripheral device has access to the peripheral bus, and thus, multiplexers are not utilized by the Riley and not inherent as suggested by the office action. Instead, Riley specifically teaches away from the use of multiplexers as claimed because the IOCC provides the functionality without the added circuitry of the multiplexers. Thus, the applied combination does not

teach or suggest, and instead teaches away from the buffers and multiplexers as recited in claim 60, and as such, claim 60 is patentable over the applied combination.

Claim 61 depends from claim 60, and thus, is patentable over the applied combination due at least to its dependency on allowable claims. Further, the applied references fail to teach or suggest a "circuit that receives computer network communication signals further comprises a first video processor; and the buffer logic circuit comprises a second video processor that receives the digital signals from the circuit that receives wireless television communication signals and forwards the digital signals to the circuit that receives computer network communication signals" as recited in claim 60. There is no suggestion or teaching in the applied references to provide a video process in the buffer logic circuit as well as in the circuit that receives the computer network communications signals. Therefore, claim 60 is also patentable over the applied combinations of references.

Claim 62 depends from claim 61 and further provides that the buffer logic circuit includes a multiplexer that and directs the digital signals to one of the first and second video processors. There is no discussion or suggestion in the applied combinations to provide a buffer logic circuit with a multiplexer that directs digital signals received from the circuit that receives television communication signals, or a multiplexer that directs the digital signals to one of a video processor in the buffer logic and a video processor in the circuit that receives computer network communication signals. Therefore, claim 61 is also patentable over the applied combinations.

Similarly, claim 63 depends from claim 62 and thus is patentable. Further, there is no discussion or suggestion in the applied references to provide buffer logic circuit that receives broadcast data in addition to the digital signals received from the circuit that receives wireless television communication signals, or that the third multiplexer forwards the signals to the first and second video processors as recited in claim 62. Therefore, claim 62 is patentable over the applied references.

Claim 64 depends from independent claim 23. As demonstrated above, claim 23 is allowable over the applied combination, and thus, claim 64 is also allowable

due at least to the dependency on claim 23. Further, claim 64 includes language similar to that of new claim 60. The applied combination of Dillon, Naiff, Legall and Riley fail to teach or suggest, for example, the multiplexing through first and second multiplexers, and buffering through first and second narrowband buffers and third wideband buffer, similar to that recited in claim 60. Therefore, the arguments presented above with respect to claim 60 can similarly be applied to claim 64. Additionally, one skilled in the art would not combine at least Dillon with Riley as demonstrated above, as such combination would require added complexity with no benefit as the Dillon patent provides already provides the satellite communications to the CPU of the personal computer without the need of the added complexity of bus buffers as described in Riley. Therefore, claim 64 is patentable over the applied combination.

Claim 65 provides that the buffer logic circuit further receives additional broadcast data and the multiplexer forwards the portion of the sensory data and the broadcast data to the first and second video processors. There is no teaching or suggestion in the applied references that a buffer logic circuit receives additional broadcast data or that a multiplexer forwards the two signals to video processors as claimed. Therefore, claim 63 is also patentable over the applied references.

CONCLUSION

Applicants submit that the above remarks demonstrate that the pending claims are in a condition for allowance. Therefore, a Notice of Allowance is respectfully requested.

Respectfully submitted,

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